What Is Claimed Is:

1. A method for supporting directory-based cache coherence in an object-addressed memory hierarchy in a computer system, comprising:

receiving a cache-coherence transaction for a cache line;

if the cache line is an object-addressed cache line, using a corresponding object identifier and offset to look up directory information specifying where copies of the object-addressed cache line are located in the caches in the computer system; and

using the directory information to perform the cache-coherence transaction.

2. The method of claim 1, wherein if the cache line is a physically-addressed cache line, the method further comprises using a corresponding physical address to look up directory information specifying where copies of the physically-addressed cache line are located in the caches.

3. The method of claim 1, wherein the method is performed by a memory controller that resides between main memory and caches in the computer system.

4. The method of claim 1, wherein looking up the directory information involves looking up the directory information in main memory.

5. The method of claim 1,

wherein directory information for a physically-addressed cache line is located alongside a corresponding physical cache line in main memory; and

wherein directory information for multiple object-addressed cache lines can be stored in a single physical cache line in main memory.

6. The method of claim 1, wherein when directory information for a given cache line is replaced by directory information for another cache line or is otherwise removed, the method further comprises flushing and/or invalidating any copies of the given cache line that are located in caches in the computer system.

7. The method of claim 1, wherein using the corresponding object identifier and offset to look up the directory information in memory involves performing a hash lookup.

8. The method of claim 1, wherein the memory controller includes a translator that translates between object identifiers (used to reference objects in an object cache) and physical addresses (used to address objects in main memory).

9. The method of claim 8,

wherein prior to receiving a request to access an object at the translator, the request is initially directed to the object cache;

wherein if the request causes a hit in the object cache, the object is accessed in the object cache and the request is not sent to the translator; and

wherein if the request causes a miss in the object cache, the request is sent to the translator.

10. The method of claim 1, wherein the cache-coherence transaction can involve:

a store to the cache line;

a load from the cache line;

an invalidation of the cache line; or

any other change in a cache-coherence-related state of the cache line.

11. The method of claim 1, wherein the caches include one or more levels of caches.

12. The method of claim 1, wherein object-addressed cache lines are used to store objects defined within an object-oriented programming system.

13. An apparatus that supports directory-based cache coherence in an object-addressed memory hierarchy in a computer system, comprising:

a receiving mechanism configured to receive a cache-coherence transaction for a cache line;

a lookup mechanism, wherein if the cache line is an object-addressed cache line, the lookup mechanism is configured to use a corresponding object identifier and offset to look up directory information specifying where copies of the object-addressed cache line are located in the caches; and

a cache-coherence mechanism configured to use the directory information to perform the cache-coherence transaction.

14. The apparatus of claim 13, wherein if the cache line is a physically-addressed cache line, the lookup mechanism is configured to use a corresponding physical address to look up directory information specifying where copies of the physically-addressed cache line are located in the caches.

15. The apparatus of claim 13, wherein the receiving mechanism, the lookup mechanism and the cache coherence mechanism are located within a memory controller that resides between main memory and caches in the computer system.

16. The apparatus of claim 13, wherein the lookup mechanism is configured to look up the directory information in main memory.

17. The apparatus of claim 13,

wherein directory information for a physically-addressed cache line is located alongside a corresponding physical cache line in main memory; and

wherein directory information for multiple object-addressed cache lines can be stored in a single physical cache line in main memory.

18. The apparatus of claim 13, further comprising an invalidation mechanism, wherein when directory information for a given cache line is replaced by directory information for another cache line or is otherwise removed, the invalidation mechanism is configured to flush and/or invalidate any copies of the given cache line that are located in caches in the computer system.

19. The apparatus of claim 13, wherein the lookup mechanism is configured to use the corresponding object identifier and offset to perform a hash lookup to obtain the directory information.

20. The apparatus of claim 13, wherein the memory controller includes a translator that translates between object identifiers (used to reference objects in an object cache) and physical addresses (used to address objects in main memory).

21. The apparatus of claim 20, further comprising an object cache;

wherein the request is initially directed to the object cache;

wherein if the request causes a hit in the object cache, the apparatus is configured to access the object in the object cache and is configured not to send the request to the translator; and

wherein if the request causes a miss in the object cache, the apparatus is configured to send the request to the translator.

22. The apparatus of claim 13, wherein the cache-coherence transaction can involve:

a store to the cache line;

a load from the cache line;

an invalidation of the cache line; or

any other change in a cache-coherence-related state of the cache line.

23. The apparatus of claim 13, wherein the caches include one or more levels of caches.

24. The apparatus of claim 13, wherein object-addressed cache lines are used to store objects defined within an object-oriented programming system.

25. A computer system that supports directory-based cache coherence in an object-addressed memory hierarchy, comprising:

one or more processors;

a set of caches coupled to the one or more processors;

a main memory;

a memory controller that couples together the set of caches and the main memory;

a receiving mechanism within the memory controller configured to receive a cache-coherence transaction for a cache line;

a lookup mechanism within the memory controller,

wherein if the cache line is an object-addressed cache line, the lookup mechanism is configured to use a corresponding object identifier and offset to look up directory information specifying where copies of the object-addressed cache line are located in the caches, and

wherein if the cache line is a physically-addressed cache line, the lookup mechanism is configured to use a corresponding physical address to look up directory information specifying where copies of the physically-addressed cache line are located in the caches; and

a cache-coherence mechanism configured to use the directory information to perform the cache-coherence transaction.